In re MICHELSON ET AL., Application No. 09/984,201
Amendment B

Amendments to the Claims:

The listing of clams will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-9 (canceled)

Claim 10 (original): A method for updating a data structure, the method comprising:

receiving a barrier bit;

receiving a start bit;

resetting a current data structure address to a predetermined address within the data structure in response to receiving the barrier bit and receiving the start bit;

receiving a plurality of data units;

updating the current data structure based on the received plurality of data units; and

advancing the current data structure address to a next location for storing a data unit.

Claim 11 (original): The method of claim 10, wherein identifying the barrier phase transition includes maintaining a current barrier state, and receiving a new barrier state indication different than the current barrier state.

Claim 12 (original): The method of claim 10, further comprising maintaining a current barrier bit state and comparing the current barrier bit state with a value of the received barrier bit.

Claim 13 (original): The method of claim 10, wherein the plurality of data units include flow control information.

Claim 14 (original): A packet switching system performing the method of claim 10.

Claim 15 (original): A packet switching element performing the method of claim 10.

Claims 16-21 (canceled)

Claim 22 (original): An apparatus for updating a data structure, the apparatus comprising:

means for receiving a barrier bit;

means for receiving a start bit;

means for resetting a current data structure address to a predetermined address within the data structure in response to receiving the barrier bit and receiving the start bit;

means for receiving a plurality of data units;

means for updating the current data structure based on the received plurality of data units; and

means for advancing the current data structure address to a next location for storing a data unit.

Claim 23 (original): The apparatus of claim 22, comprising means for maintaining a current barrier state, and means for receiving a new barrier state indication different than the current barrier state.

Claim 24 (original): The apparatus of claim 22, comprising means for maintaining a current barrier bit state and means for comparing the current barrier bit state with a value of the received barrier bit.

Claim 25 (original): The apparatus of claim 22, wherein the plurality of data units include flow control information.

Claim 26 (original): A packet switching system comprising:

a plurality of first elements;

a plurality of second elements;

wherein each of the plurality of first elements includes:

a memory configured to store a first data structure;

a first barrier state maintainer to indicate a current first barrier state;

a first barrier accumulator to receive indications of a first subset of a plurality of barrier request messages, to determine when a first barrier request may be sent to the plurality of second elements, and to update the current first barrier state; and

a first data forwarder for sending information maintained in the first data structure to the plurality of second elements.

Claim 27 (original): The packet switching system of claim 26, wherein each of the plurality of second elements includes:

a second memory configured to store a second data structure;

a second barrier state maintainer to indicate a current second barrier state;

a second barrier accumulator to receive indications of a second subset of a plurality of barrier request messages, to determine when a second barrier request may be sent to a plurality of third elements, and to update the current second barrier state; and

a second data forwarder for sending information maintained in the second data structure in a predetermined order to the plurality of third elements,

wherein the predetermined order is reset in response to identifying a barrier state transition.

Claim 28 (original): The packet switching system of claim 27, wherein each of the plurality of third elements includes:

a third memory configured to store a third data structure;

a third barrier state maintainer to indicate a current third barrier state;

a third barrier accumulator to receive indications of a third subset of a plurality of barrier request messages, to determine when a third barrier request may be sent, and to update the current third barrier state.

Claim 29 (original): The packet switching system of claim 26, wherein each of the plurality of second elements includes a second data forwarder for sending said first data structure information received from the plurality of first elements to a plurality of third elements.

Claim 30 (previously presented): The packet switching system of claim 29, wherein each of the plurality of first elements, the plurality of second elements, and the plurality of third elements is a switching element.

Claim 31 (currently amended): The packet switching system of claim 26, wherein each of the plurality of first elements is a switching element.

Claim 32 (previously presented): The packet switching system of claim 31, wherein each of the plurality of second elements is a switching element.

Claim 33-36 (canceled)